What is claimed is :

1. A semiconductor device comprising an insulating film structure which electrically insulates a conductive region from a silicon region, wherein said insulating film structure extends on said silicon region and under said conductive region, said insulating film structure further comprising at least one silicate region composed of a silicon oxide containing at least one metal element subjected to thermal diffusion.

2. The semiconductor device according to claim 1, wherein concentration distribution of said at least one metal element in said silicate region is distribution derived from thermal diffusion.

3. The semiconductor device according to claim 1, wherein said insulating film structure comprises at least one silicon oxide region composed of a silicon oxide not containing said at least one metal element, at least one metal rich region having high concentration of said at least one metal element, and said at least one silicate region which is located between said silicon oxide region and said metal rich region and has lower concentration of said at least one metal element than that of said metal rich region.

4. The semiconductor device according to claim 3, wherein said silicate region has composition modulation in which composition of said at least one metal element increases as closer to said metal rich region and decreases as closer to said silicon oxide region, and, on the contrary, in which the composition of silicon decreases as closer to said metal rich region and increases as closer to said silicon oxide region.

5. The semiconductor device according to claim 3, wherein said metal rich region comprises a metal oxide not containing silicon.

6. The semiconductor device according to claim 3,

wherein said metal rich region comprises metal rich silicate having higher concentration distribution of said at least one metal element than that of said silicate region.

7. The semiconductor device according to claim 3,

wherein said silicon oxide region is located on said silicon region, said silicate region being located on said silicon oxide region, said metal rich region being located on said silicate region.

8. The semiconductor device according to claim 7,

wherein said silicate region has composition modulation in which composition of said at least one metal element increases toward a surface of the device, and the composition of silicon decreases toward the surface of the device.

9. The semiconductor device according to claim 8,

wherein a second silicate region further extends on said metal rich region, the second silicate region having composition modulation in which composition of said at least one metal element decreases upward, and the composition of silicon increases upward.

10. The semiconductor device according to claim 1,

wherein said silicon region comprises a silicon substrate, said conductive region comprises a gate electrode, and said insulating film structure comprises a gate insulating film.

11. The semiconductor device according to claim 1,

wherein said at least one metal element is at least any one selected from a group of Zr, Hf, Ta, Al, Ti, Nb, Sc, Y, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and Lu.

12. The semiconductor device according to claim 1,

wherein a source of said at least one metal element subjected to thermal diffusion comprises a metal layer deposited on a surface of a base silicon oxide film extending on said silicon region in atmosphere with residual oxygen partial pressure of 1×10^{-6} Torr or less.

13. The semiconductor device according to claim 1,

wherein a source of said at least one metal element subjected to thermal diffusion comprises a metal layer deposited on a surface of a base silicon oxide film extending on said silicon region by causing temperature rise of said silicon region from room temperature.

14. The semiconductor device according to claim 1,

wherein a source of said at least one metal element subjected to thermal diffusion comprises a metal layer having a film thickness of 1 nm or less.

15. The semiconductor device according to claim 1,

wherein a source of said at least one metal element subjected to thermal diffusion comprises a metal layer having a film thickness of 0.6 nm or less.

16. The semiconductor device according to claim 1,

wherein said at least one metal element is only Al, and a source of the metal element comprises a metal layer abutting on a surface of a base silicon oxide film having a film thickness of not less than 0.6 nm, which extends on said silicon region.

17. The semiconductor device according to claim 1,

wherein said at least one metal element comprises at least only any one selected from a group of Zr, Hf, Ta, Al, Ti, Nb, Sc, Y, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and Lu, and

a source of the metal element comprises a metal layer abutting on a surface of a base silicon oxide film having a film thickness of not less than 1 nm, which extends on said silicon region.

18. The semiconductor device according to claim 1,

wherein said insulating film structure up to and including its uppermost portion is composed of silicate containing said at least one metal element subjected to thermal diffusion.

19. The semiconductor device according to claim 1, wherein said insulating film structure does not include an unreacted metal region not containing silicon.

20. The semiconductor device according to claim 19, wherein said unreacted metal region comprises a region which is removed by at least any one of a hydrofluoric acid solution and an ammonia peroxide solution.

21. The semiconductor device according to claim 19, wherein said insulating film structure has film quality reformed as a result of heat treatment in a state where said unreacted metal region is not present.

22. The semiconductor device according to claim 1, wherein said insulating film structure comprises at least both of a first silicate region composed of a silicon oxide containing at least one metal element subjected to thermal diffusion, and a second silicate region which is located above the first silicate region and is composed of a silicon-containing insulator containing said at least one metal element subjected to thermal diffusion.

23. The semiconductor device according to claim 22, wherein said silicon-containing insulator comprises any one selected from a group of a silicon oxide film, a silicon oxynitride film, a silicon nitride film, and a laminated structure of at least two from the silicon oxide film, the silicon oxynitride film, and the silicon nitride film.

24. The semiconductor device according to claim 22, wherein said first silicate region comprises a base silicon oxide film containing said at least one metal element subjected to thermal diffusion from a metal layer abutting on an upper surface, and said second silicate region comprises a cap layer of a silicon-containing insulator containing said at least one metal element thermally diffused from said metal layer abutting on a lower surface.

25. The semiconductor device according to claim 24, wherein a film thickness of said cap layer is 1 nm or less

26. The semiconductor device according to claim 23, wherein a film thickness of said cap layer is 0.5 nm or less.

27. The semiconductor device according to claim 22, wherein said insulating film structure has composition modulation in which composition of silicon in a film thickness direction is high in the lowermost portion and uppermost portion, which are located in the vicinity of said silicon region, and low in the central portion.

28. The semiconductor device according to claim 22, wherein said insulating film structure has composition modulation in which composition of said at least one metal element in a film thickness direction is low in the lowermost portion and uppermost portion, which are located in the vicinity of said silicon region, and high in the central portion.

29. The semiconductor device according to claim 1, wherein an Equivalent Oxide Thickness of said insulating film structure is smaller than the Equivalent Oxide Thickness of a silicon oxide film into which said at least one metal element is diffused.

30. The semiconductor device according to claim 1, wherein said silicon oxide constituting said at least one silicate region is a silicon oxynitride into which nitrogen is introduced.

31. The semiconductor device according to claim 1, wherein concentration distribution of said at least one metal element in said at least one silicate region is a distribution derived from heat treatment under reduced oxygen pressure conditions below atmospheric pressure.

32. The semiconductor device according to claim 1,

wherein said insulating film structure further comprises a cap region composed of any one of a silicon nitride and a silicon oxynitride on said at least one silicate region.

33. The semiconductor device according to claim 32,
wherein a thickness of said cap region is 0.5 nm or less.

34. The semiconductor device according to claim 1,
wherein said conductive region comprises a gate electrode, and said insulating film structure comprises a gate insulating film, and
wherein a hysteresis width of C-V characteristics is 5 mV or less for a gate bias within device operating voltage.

35. The semiconductor device according to claim 1,
wherein said insulating film structure comprises said silicate region composed of a silicon oxide containing said at least one metal element, and a silicon oxide region composed of a silicon oxide not containing a metal element,
wherein a physical film thickness of said insulating film structure is 3.5 nm or less, and a physical thickness of said silicate region is thinner than the physical thickness of said silicon oxide region.

36. The semiconductor device according to claim 35,
wherein a physical thickness of said silicate region is 1.5 nm or less.

37. The semiconductor device according to claim 35,
wherein said conductive region comprises a gate electrode, said insulating film structure comprises a gate insulating film, and the gate electrode has nitride film side walls.

38. A manufacturing method of a semiconductor device comprising an insulating film structure which electrically insulates a conductive region from a silicon region,
wherein the manufacturing method further comprising at least steps of:
forming a base silicon oxide film on said silicon region;
forming a metal layer on said base silicon oxide film; and

forming the insulating film structure,
wherein the insulating film structure is formed by giving heat treatment to cause a silicate reaction in an interface between said base silicon oxide film and said metal layer to allow thermal diffusion of at least one metal element contained in said metal layer into said base silicon oxide film to thereby form the insulating film structure including a silicate region composed of a silicon oxide containing said at least one metal element thermally diffused in a region of at least part of said base silicon oxide film.

39. The manufacturing method of a semiconductor device according to claim 38,
wherein said heat treatment causing said interface silicate reaction is carried out in reducing atmosphere.

40. The manufacturing method of a semiconductor device according to claim 38,
wherein said heat treatment causing said interface silicate reaction is carried out in atmosphere containing any one of hydrogen and ammonia.

41. The manufacturing method of a semiconductor device according to claim 38,
wherein said thermal diffusion forms said insulating film structure comprising at least one silicon oxide region composed of a silicon oxide into which said at least one metal element is not diffused, at least one metal rich region into which said at least one metal element has been diffused at high concentration, and said at least one silicate region which is located between said silicon oxide region and said metal rich region, and into which said at least one metal element has been diffused at concentration lower than that of said metal rich region.

42. The manufacturing method of a semiconductor device according to claim 41,
wherein said silicate region has composition modulation in which composition of said at least one metal element increases as closer to said metal rich region and decreases as closer to said silicon oxide region, and, on the other hand, in which the composition of silicon decreases as closer

to said metal rich region and increases as closer to said silicon oxide region.

43. The manufacturing method of a semiconductor device according to claim 41,
wherein said metal rich region comprises a metal oxide not containing silicon.

44. The manufacturing method of a semiconductor device according to claim 41,
wherein said metal rich region comprises metal rich silicate having higher concentration distribution of said at least one metal element than that of said silicate region.

45. The manufacturing method of a semiconductor device according to claim 38,
wherein a process of forming said metal layer comprises a deposition process carried out by setting residual oxygen partial pressure in treatment atmosphere to 1×10^{-6} Torr or less.

46. The manufacturing method of a semiconductor device according to claim 38,
wherein a deposition process of said metal layer is carried out by causing temperature rise of said silicon region from room temperature.

47. The manufacturing method of a semiconductor device according to claim 38,
wherein a nitrization process is further carried out subsequent to said heat treatment process.

48. The manufacturing method of a semiconductor device according to claim 47,
wherein said nitrization process comprises heat treatment in ammonia.

49. The manufacturing method of a semiconductor device according to claim 47,

wherein said nitride treatment process comprises nitrogen plasma treatment.

50. The manufacturing method of a semiconductor device according to claim 38,
wherein said at least one metal element is at least any one selected from a group of Zr, Hf, Ta, Al, Ti, Nb, Sc, Y, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and Lu.

51. The manufacturing method of a semiconductor device according to claim 38,
wherein said at least one metal element is only Al, and said base silicon oxide film is formed with a film thickness of not less than 0.6 nm.

52. The manufacturing method of a semiconductor device according to claim 38,
wherein said at least one metal element contains at least any one selected from a group of Zr, Hf, Ta, Al, Ti, Nb, Sc, Y, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and Lu, and said base silicon oxide film is formed with a film thickness of not less than 1 nm.

53. The manufacturing method of a semiconductor device according to claim 38,
wherein a forming process of said metal layer is carried out on condition that a film thickness of metal deposition is 1 nm or less.

54. The manufacturing method of a semiconductor device according to claim 38,
wherein a forming process of said metal layer is a process carried out on condition that a film thickness of metal deposition is 0.6 nm or less.

55. The manufacturing method of a semiconductor device according to claim 38,
wherein said heat treatment process is carried out for a silicate reaction in an interface between said metal layer and said base silicon oxide film to progress to an upper portion of said metal layer, thereby forming said

insulating film structure up to and including its uppermost portion from silicate.

56. The manufacturing method of a semiconductor device according to claim 38, the manufacturing method further comprising a step of:
removing an unreacted metal region subsequent to said heat treatment process, when the unreacted metal region is left in said metal layer by said heat treatment process.

57. The manufacturing method of a semiconductor device according to claim 56,
wherein a process of removing said unreacted metal region is carried out by use of a hydrofluoric acid solution or an ammonia peroxide solution.

58. The manufacturing method of a semiconductor device according to claim 56, further comprising a heat treatment process for reforming film quality subsequent to a process of removing said unreacted metal region.

59. The manufacturing method of a semiconductor device according to claim 38, the manufacturing method further comprising a step of:
depositing a cap layer composed of a silicon-containing insulating film on said metal layer after a formation process of said metal layer and before said heat treatment process to thereby allow said silicate reaction to cause thermal diffusion of said at least one metal element into said base silicon oxide film and said cap layer to thereby form a first silicate layer composed of a silicon oxide containing said at least one metal element thermally diffused in a region of at least part of said base silicon oxide film, as well as to form a second silicate layer composed of a silicon insulator containing said at least one metal layer thermally diffused in a region of at least part of said cap layer.

60. The manufacturing method of a semiconductor device according to claim 59,
wherein said cap layer comprises any one selected from a group of a silicon oxide film, a silicon oxynitride film, a silicon nitride film, and a laminated

structure of at least two from the silicon oxide film, the silicon oxynitride film, and the silicon nitride film.

61. The manufacturing method of a semiconductor device according to claim 59,
wherein a film thickness of said cap layer is 1 nm or less.

62. The manufacturing method of a semiconductor device according to claim 59,
wherein a film thickness of said cap layer is 0.5 nm or less.

63. The manufacturing method of a semiconductor device according to claim 38,
wherein said insulating film structure has composition modulation in which composition of silicon in a film thickness direction is high in the lowermost portion and uppermost portion, which are located in the vicinity of said silicon region, and low in the central portion.

64. The manufacturing method of a semiconductor device according to claim 38,
wherein said insulating film structure has composition modulation in which composition of said at least one metal element in a film thickness direction is low in the lowermost portion and uppermost portion, which are located in the vicinity of said silicon region, and high in the central portion.

65. The manufacturing method of a semiconductor device according to claim 38,
wherein an Equivalent Oxide Thickness of said insulating film structure is smaller than the Equivalent Oxide Thickness of said base silicon oxide film.

66 The manufacturing method of a semiconductor device according to claim 38,
wherein said base silicon oxide film comprises a silicon oxynitride film into which nitrogen is introduced.

67. The manufacturing method of a semiconductor device according to claim 38,
wherein said heat treatment process is carried out under reduced oxygen pressure conditions below atmospheric pressure.

68. The manufacturing method of a semiconductor device according to claim 38,
wherein said silicon region comprises a silicon substrate, said conductive region comprises a gate electrode, and said insulating film structure comprises a gate insulating film.

69. A manufacturing apparatus of a semiconductor device having a gate insulating film which electrically insulates a gate electrode from a silicon substrate, the manufacturing apparatus comprising:

a deposition chamber introducing said silicon substrate in which a base silicon oxide film is formed;

a metal evaporation unit by which a metal layer is deposited on said base silicon oxide film of said silicon substrate introduced into the deposition chamber; and

an vacuum pump controlling residual oxygen partial pressure in said deposition chamber,

wherein said metal evaporation unit allows said vacuum pump to make the residual oxygen partial pressure in said deposition chamber 1 x 10^{-6} Torr or less to deposit said metal layer on said base silicon oxide film.

70. A manufacturing apparatus of a semiconductor device according to claim 69, further comprising a substrate heating unit by which said silicon substrate introduced into said deposition chamber is heated.

71. The manufacturing apparatus of a semiconductor device according to claim 69,
wherein said metal evaporation unit allows a spacing between an evaporation source and a substrate to be set to not less than 100 mm to deposit said metal layer on said base silicon oxide film.